FIG. 1

PHASE	CODE	BLOCK PAYLOAD
0	I_0	i_0, i_0, i_0, i_0
1	I_1	i_0, i_0, i_0, i_1
2	I_2	i_0, i_0, i_1, i_0
3	I_3	i_0, i_0, i_1, i_1
4	I_4	i_0, i_1, i_0, i_0
5	I_5	i_0, i_1, i_0, i_1
6	I_6	i_0, i_1, i_1, i_0
7	I_7	i_0, i_1, i_1, i_1
8	I_8	i_1, i_0, i_0, i_0
9	I_9	i_1, i_0, i_0, i_1
10	I_{10}	i_1, i_0, i_1, i_0
11	I_{11}	i_1, i_0, i_1, i_1
12	I_{12}	i_1, i_1, i_0, i_0
13	I_{13}	i_1, i_1, i_0, i_1
14	I_{14}	i_1, i_1, i_1, i_0
15	I_{15}	i_1, i_1, i_1, i_1

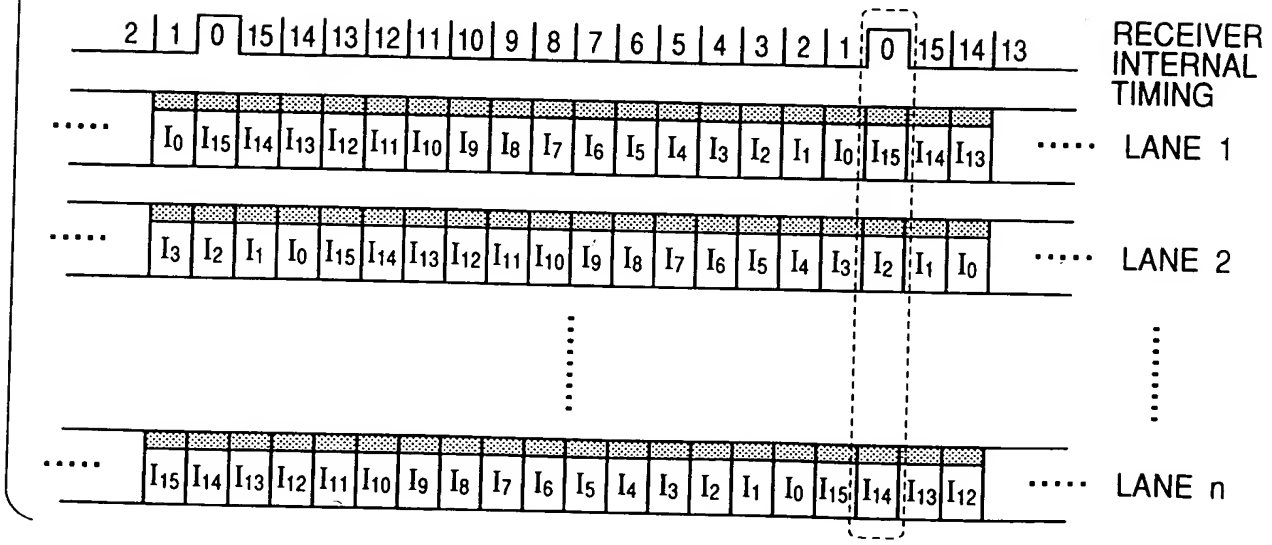


FIG. 2

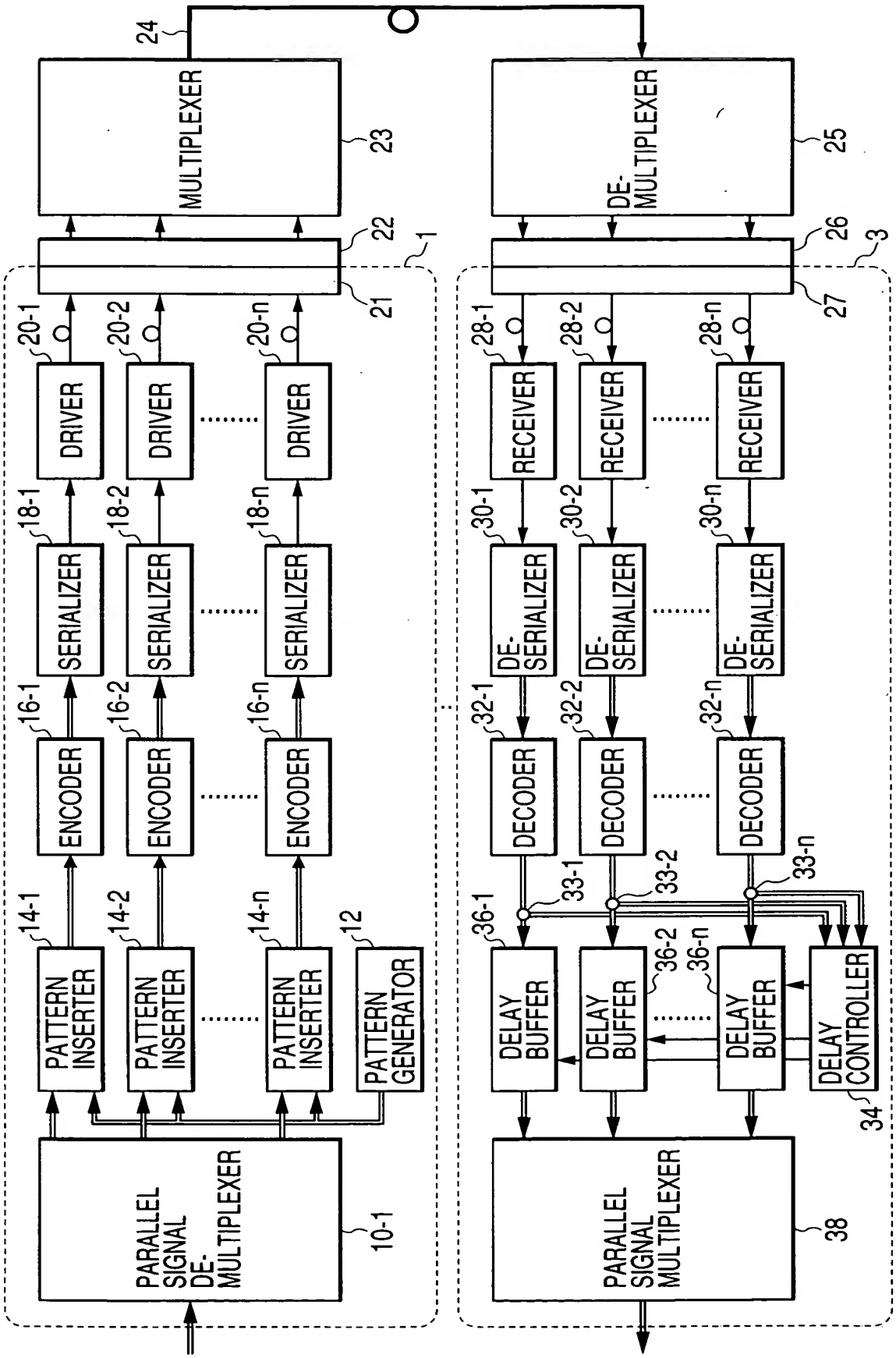

PARALLEL SIGNAL DE-MULTIPLEXER
10-1
PATTERN GENERATOR
12
PATTERN INSERTER
14-1
14-2
14-n
ENCODER
16-1
16-2
16-n
SERIALIZER
18-1
18-2
18-n
DRIVER
20-1
20-2
20-n
1
21
22
MULTIPLEXER
23
24
DE-MULTIPLEXER
25
26
27
3
RECEIVER
28-1
28-2
28-n
DE-SERIALIZER
30-1
30-2
30-n
DECODER
32-1
32-2
32-n
33-1
33-2
33-n
DELAY BUFFER
36-1
36-2
36-n
DELAY CONTROLLER
34
PARALLEL SIGNAL MULTIPLEXER
38

FIG. 3

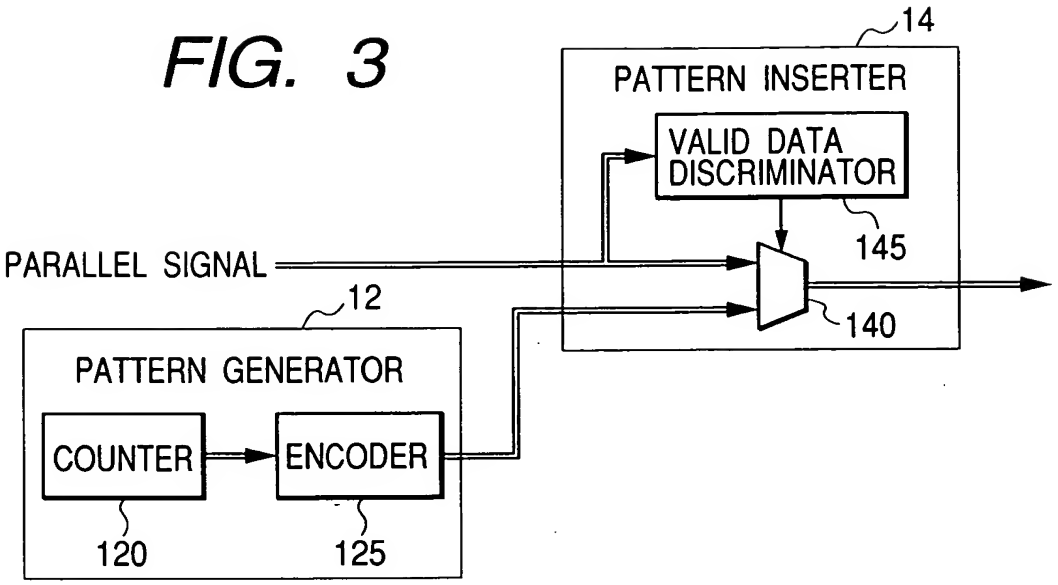

14
PATTERN INSERTER
VALID DATA DISCRIMINATOR
145
PARALLEL SIGNAL
140
12
PATTERN GENERATOR
COUNTER
ENCODER
120
125

FIG. 4

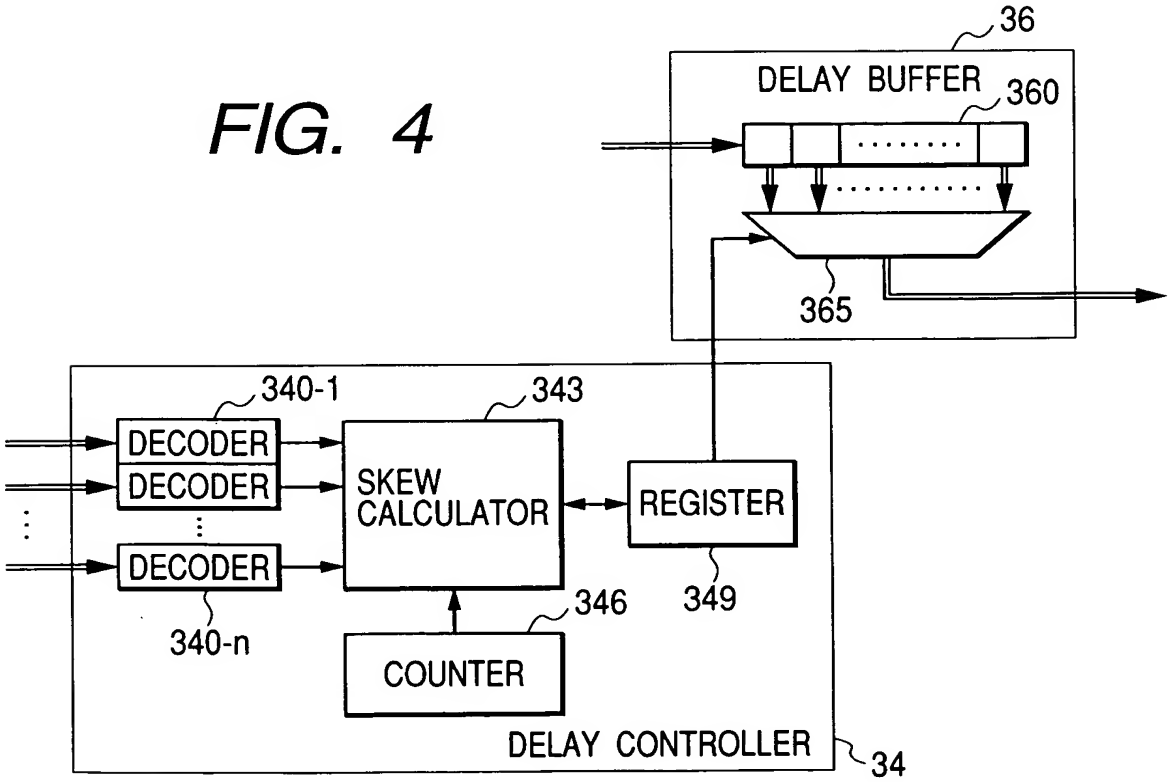

36
DELAY BUFFER
360
365
340-1
343
DECODER
DECODER
DECODER
SKEW CALCULATOR
REGISTER
340-n
346
349
COUNTER
DELAY CONTROLLER
34

FIG. 5

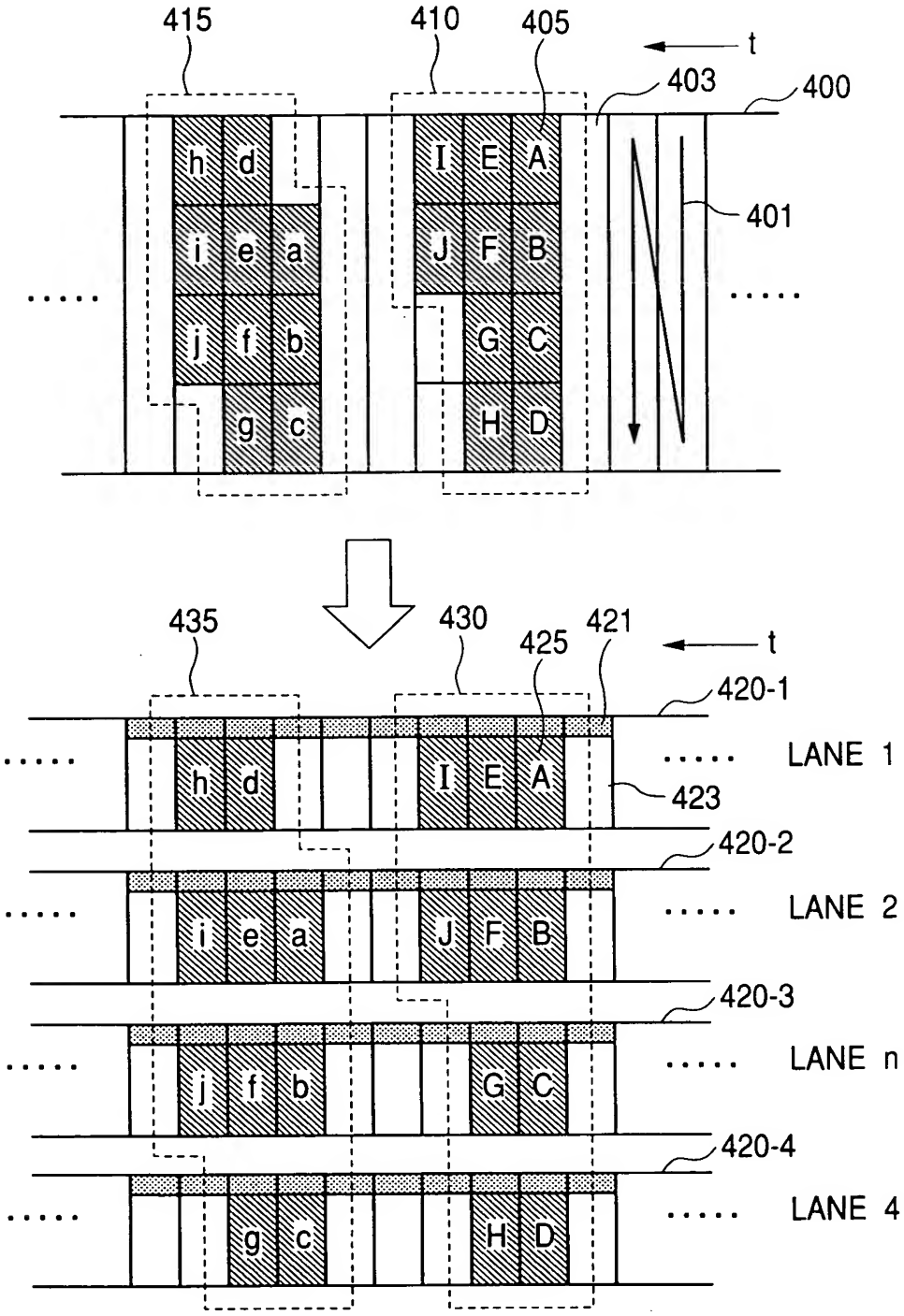

415
410
405
t
403
400
401
h
d
i
e
a
j
f
b
g
c
I
E
A
J
F
B
G
C
H
D
435
430
425
421
420-1
LANE 1
423
420-2
LANE 2
420-3
LANE n
420-4
LANE 4

FIG. 6

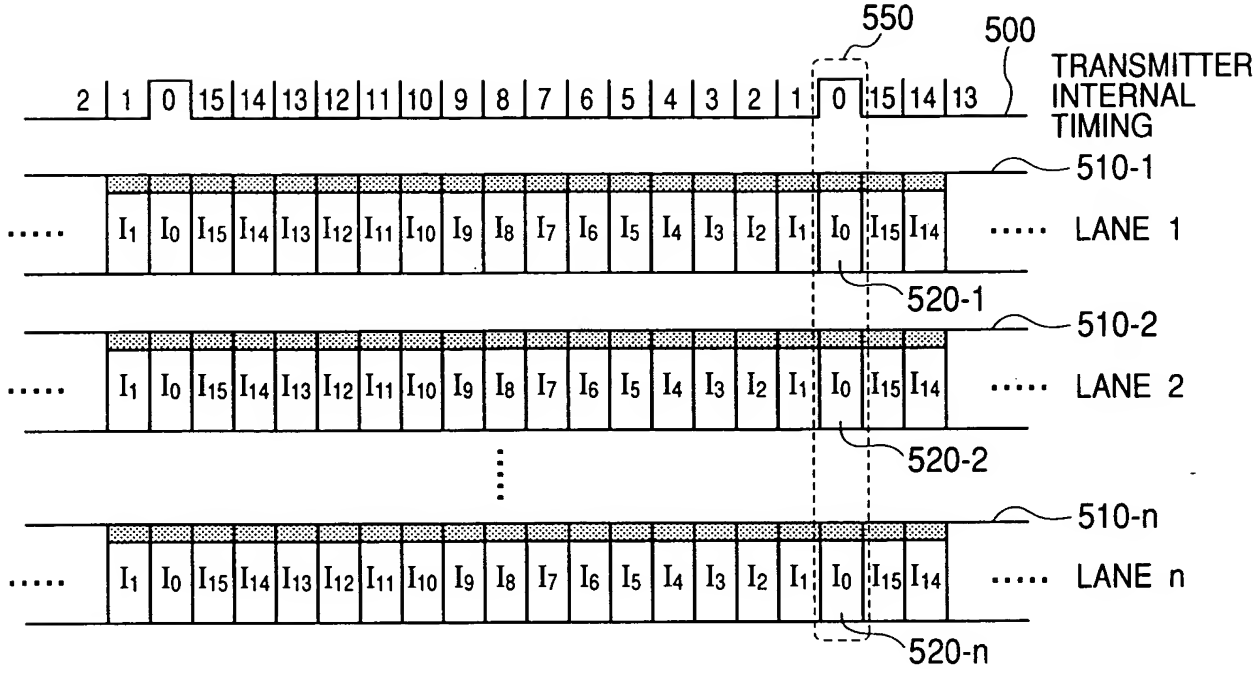

550
500
TRANSMITTER INTERNAL TIMING
510-1
LANE 1
520-1
510-2
LANE 2
520-2
510-n
LANE n
520-n

FIG. 7

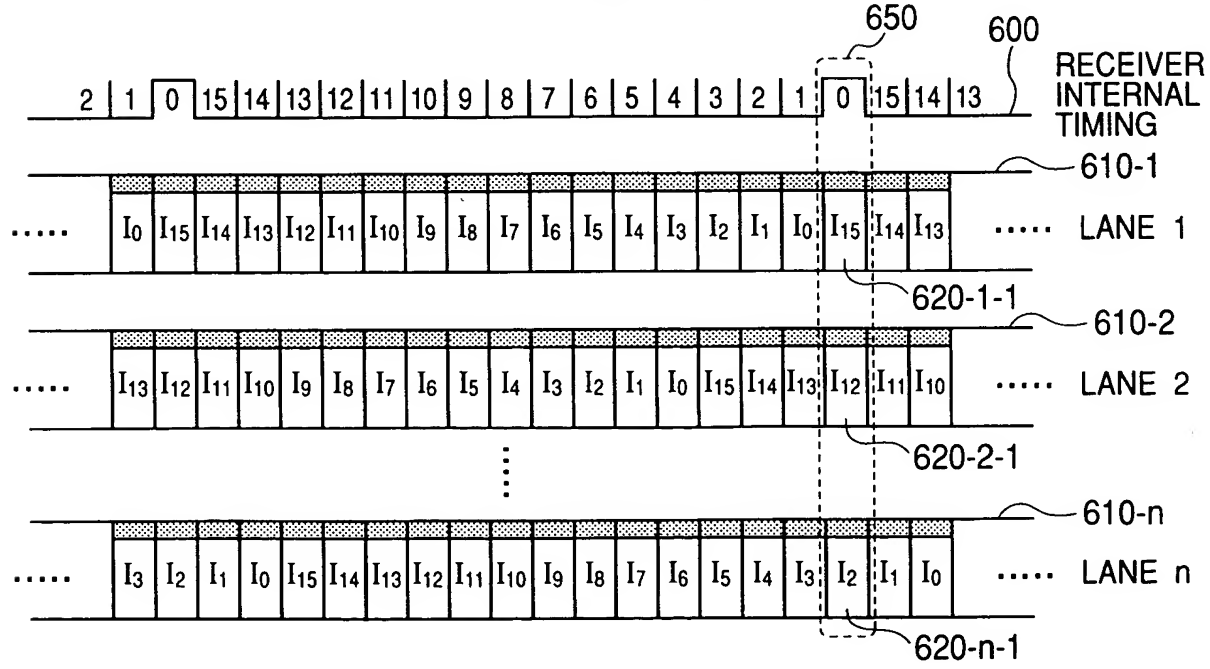

650
600
RECEIVER INTERNAL TIMING
610-1
LANE 1
620-1-1
610-2
LANE 2
620-2-1
610-n
LANE n
620-n-1

FIG. 8

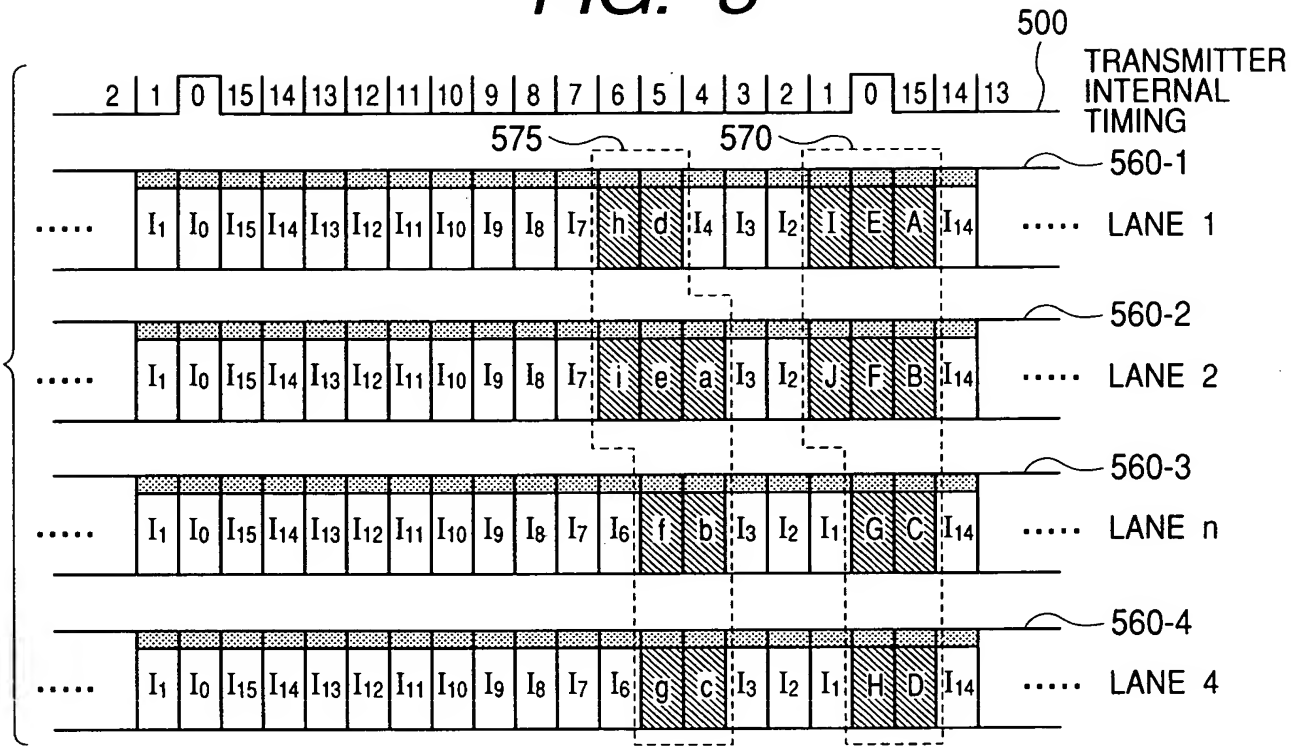

500
TRANSMITTER INTERNAL TIMING
2 1 0 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 15 14 13
575
570
560-1
LANE 1
560-2
LANE 2
560-3
LANE n
560-4
LANE 4

FIG. 9

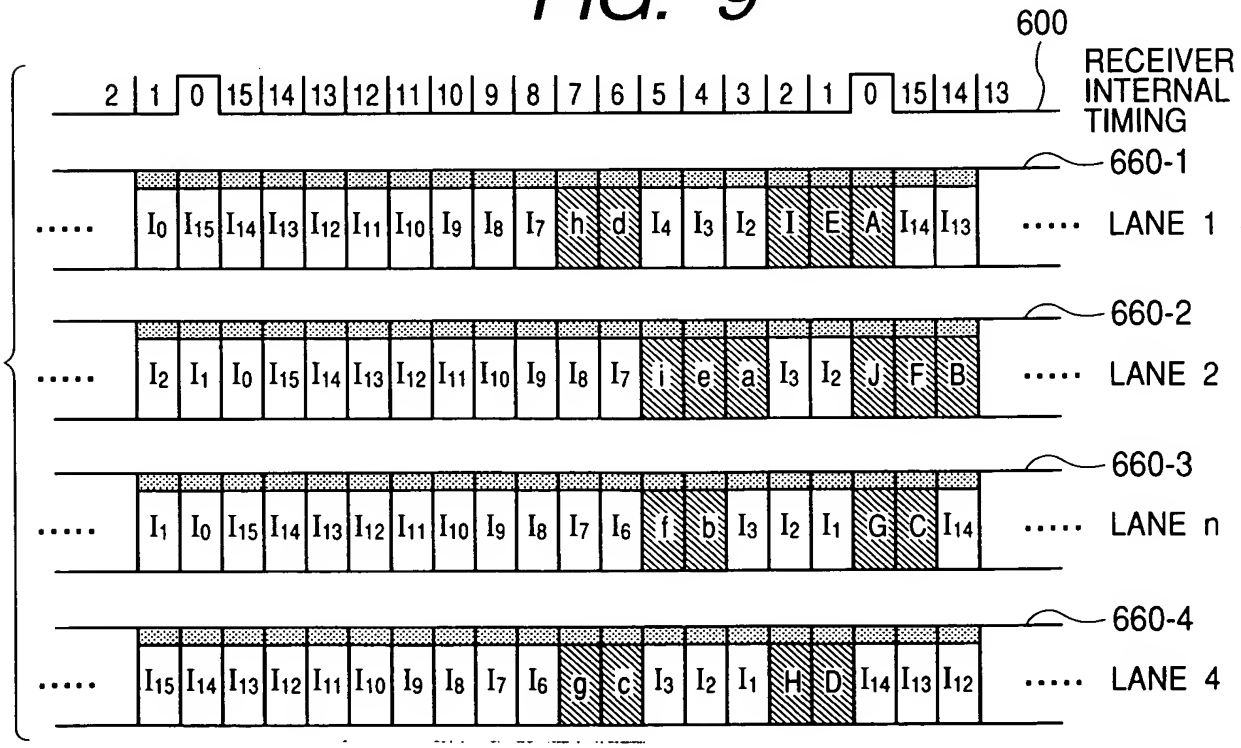
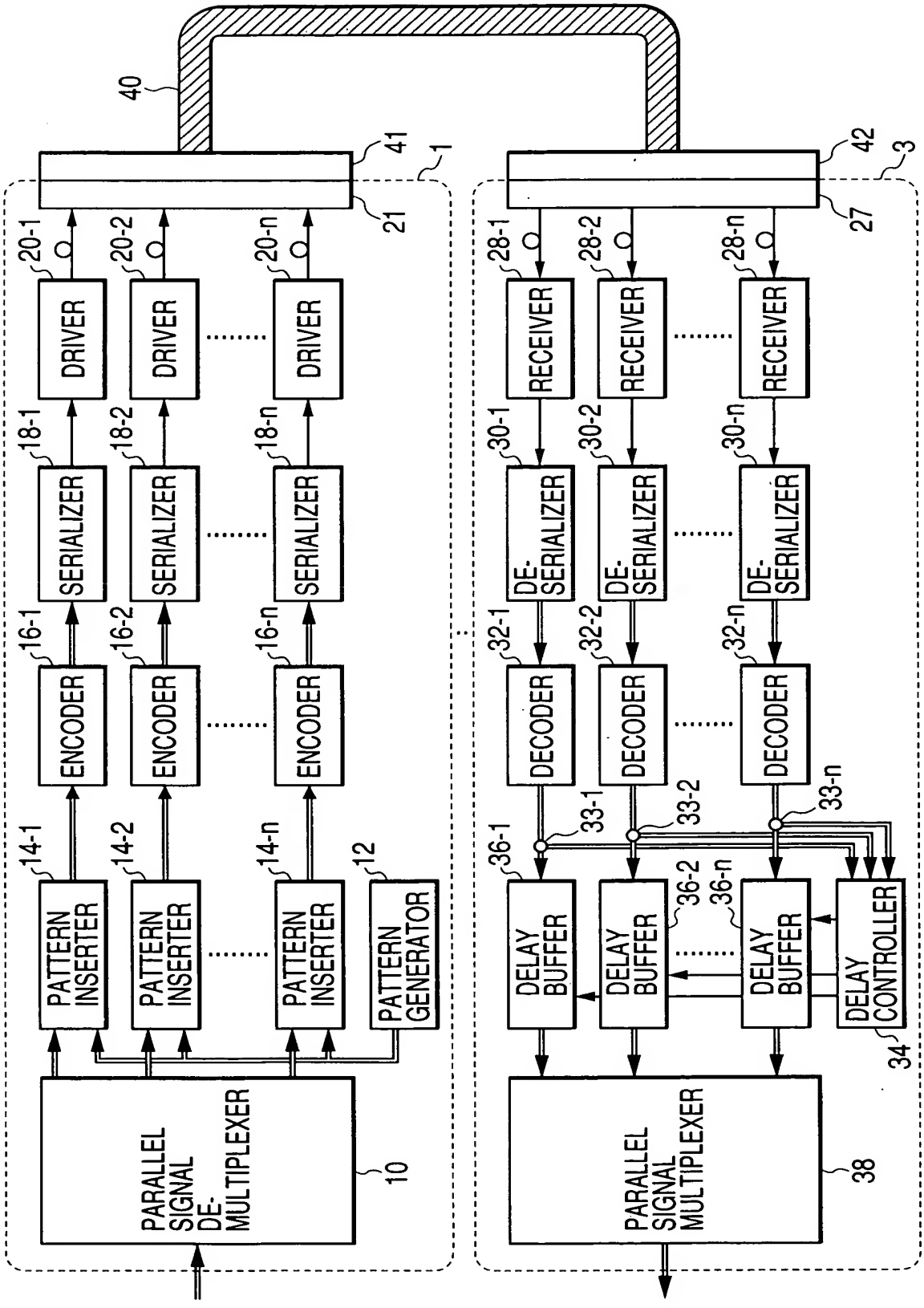

600
RECEIVER INTERNAL TIMING
2 1 0 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 15 14 13
660-1
LANE 1
660-2
LANE 2
660-3
LANE n
660-4
LANE 4

FIG. 10


40
41
1
21
42
3
27
20-1
20-2
20-n
DRIVER
18-1
18-2
18-n
SERIALIZER
16-1
16-2
16-n
ENCODER
14-1
14-2
14-n
PATTERN INSERTER
12
PATTERN GENERATOR
PARALLEL SIGNAL DE-MULTIPLEXER
10
28-1
28-2
28-n
RECEIVER
30-1
30-2
30-n
DE-SERIALIZER
32-1
32-2
32-n
DECODER
33-1
33-2
33-n
36-1
36-2
36-n
DELAY BUFFER
DELAY CONTROLLER
34
PARALLEL SIGNAL MULTIPLEXER
38